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TITLE: DAMASCENE PHASE CHANGE MEMORY

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## DAMASCENE PHASE CHANGE MEMORY

### Background

This invention relates generally to phase change memories.

Phase change memory devices use phase change materials, i.e., materials that may be electrically switched between a generally amorphous and a generally crystalline state, as an electronic memory. One type of memory element utilizes a phase change material that may be, in one application, electrically switched between generally amorphous and generally crystalline local orders or between the different detectable states of local order across the entire spectrum between completely amorphous and completely crystalline states.

Typical materials suitable for such an application include various chalcogenide elements. The state of the phase change materials is also non-volatile. When the memory is set in either a crystalline, semi-crystalline, amorphous, or semi-amorphous state representing a resistance value, that value is retained until reprogrammed, even if power is removed. This is because the program value represents a phase or physical state of the memory (e.g., crystalline or amorphous).

Thus, there is a need for better ways to form phase change memories.

#### Brief Description of the Drawings

Figure 1 is a partially schematic depiction of one  
5 embodiment of the present invention;

Figure 2 is an enlarged, cross-sectional view at an early stage of manufacture in accordance with one embodiment of the present invention;

Figure 3 is an enlarged, cross-sectional view at a  
10 subsequent stage of manufacture in accordance with one embodiment of the present invention;

Figure 4 is an enlarged, cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

15 Figure 5 is an enlarged, cross-sectional view at still a subsequent stage of manufacture in accordance with one embodiment of the present invention;

Figure 6 is an enlarged, cross-sectional view at a subsequent stage of manufacture in accordance with one  
20 embodiment of the present invention;

Figure 7 is an enlarged, cross-sectional view at a subsequent stage of one embodiment of the present invention; and

Figure 8 is a schematic system depiction in accordance  
25 with one embodiment of the present invention.

### Detailed Description

Referring to Figure 1, a phase change memory 11 may have a select device 24 that selects the phase change memory by coupling the memory to a conductive line 26 that in one embodiment may be a row line. The select device 24 may be a diode or a transistor, as two examples. Another conductive line 22 is positioned over the phase change memory device. A conductive line 22 may be a column line in one embodiment of the present invention. However, it should be understood that the designations of rows and columns are generally arbitrary.

In general, the structure depicted in Figure 1 is a cell of a phase change memory 11 that may include a large number of similarly situated cells addressable on rows and columns.

In one embodiment of the present invention, the select device 24 and the line 26 may be formed in a semiconductor substrate 10. A layer of insulating material 12 is positioned over the substrate 10. A conductive electrode 16 may form a heater that extends through a pore defined in the insulating layer 12. In one embodiment of the present invention, the electrode 16 takes up more of the available vertical extent of pore than does the phase change material 20a. The material 20a of one cell may be isolated from the phase change material of other cells.

In one embodiment, the phase change material 20a may be a non-volatile, phase change material. A phase change material may be a material having electrical properties (e.g., resistance) that may be changed through the application of energy such as, for example, heat, light, voltage potential, or electrical current.

Examples of phase change materials may include a chalcogenide material or an ovonic material. An ovonic material may be a material that undergoes electronic or structural changes and acts as a semiconductor once subjected to application of a voltage potential, electrical current, light, heat, etc. A chalcogenide material may be a material that includes at least one element from column VI of the periodic table or may be a material that includes one or more of the chalcogen elements, e.g., any of the elements of tellurium, sulfur, or selenium. Ovonic and chalcogenide materials may be non-volatile memory materials that may be used to store information.

In one embodiment, the memory material may be chalcogenide element composition from the class of tellurium-germanium-antimony ( $\text{Te}_x\text{Ge}_y\text{Sb}_z$ ) material or a GeSbTe alloy, although the scope of the present invention is not limited to just these materials.

In one embodiment, if the memory material is a non-volatile, phase change material, the memory material may be programmed into one of at least two memory states by

applying an electrical signal to the memory material. An electrical signal may alter the phase of the memory material between a substantially crystalline state and a substantially amorphous state, wherein the electrical resistance of the memory material in the substantially amorphous state is greater than the resistance of the memory material in the substantially crystalline state. Accordingly, in this embodiment, the memory material may be adapted to be altered to one of at least two resistance values within a range of resistance values to provide single bit or multi-bit storage of information.

Programming of the memory material to alter the state or phase of the material may be accomplished by applying voltage potentials to the lines 22 and 26, thereby generating a voltage potential across the memory material 20a. An electrical current may flow through a portion of the memory material 20a and for the electrode 16 in response to the applied voltage potentials, and may result in heating of the memory material 20a.

This heating and subsequent cooling may alter the memory state or phase of the memory material 20a. Altering the phase or state of the memory material 20a may alter an electrical characteristic of the memory material 20a. For example, resistance of the material 20a may be altered by altering the phase of the memory material 20a. The memory

material may also be referred to as a programmable resistive material or simply a programmable material.

5 In one embodiment, a voltage potential difference of about 3 volts may be applied across a portion of the memory material by applying about 3 volts to a lower line 26 and about zero volts to an upper line 26. A current flowing through the memory material 20a in response to the applied voltage potentials may result in heating of the memory material. This heating and subsequent cooling may alter  
10 the memory state or phase of the material.

In a "reset" state, the memory material may be in an amorphous or semi-amorphous state and in a "set" state, the memory material may be in a crystalline or semi-crystalline state. The resistance of the memory material in the  
15 amorphous or semi-amorphous state may be greater than the resistance of the material in the crystalline or semi-crystalline state. The association of reset and set with amorphous and crystalline states, respectively, is a convention. Other conventions may be adopted.

20 Due to electrical current, the memory material may be heated to a relatively higher temperature to amorphize memory material and "reset" memory material (e.g., program memory material to a logic "0" value). Heating the volume or memory material to a relatively lower crystallization  
25 temperature may crystallize memory material and "set" memory material (e.g., program memory material to a logic

"1" value). Various resistances of memory material may be achieved to store information by varying the amount of current flow and duration through the volume of memory material.

5       The information stored in memory material 20a may be read by measuring the resistance of the memory material. As an example, a read current may be provided to the memory material using opposed lines 22, 26 and a resulting read voltage across the memory material may be compared against  
10 a reference voltage using, for example, a sense amplifier (not shown). The read voltage may be proportional to the resistance exhibited by the memory storage element. Thus, a higher voltage may indicate that memory material is in a relatively higher resistance state, e.g., a "reset" state.  
15 A lower voltage may indicate that the memory material is in a relatively lower resistance state, e.g., a "set" state.

Referring to Figure 2, a damascene process may be utilized to form the phase change memory in accordance with one embodiment of the present invention. A damascene  
20 process is an integrated circuit process by which a pattern is embedded in a dielectric film on a substrate. Initially, over a substrate 10 that may define a select device 24 and a conductor 26, an insulator 12 may be defined. A pore or aperture 14 may be formed through the  
25 insulating layer 12, for example, using conventional masking and etching techniques.

The aperture 14 may then be filled with a suitable electrode 16. The electrode 16 may be any of a variety of materials utilized for electrodes or heaters for phase change memories, such as metallic materials including tungsten, titanium nitride, and titanium silicon nitride. Any metal can be used, but for heating more resistive metals may be used. Suitable materials in some embodiments may include materials that have high resistivity and low thermal conductivity. The material 16 may be deposited into the aperture 14 and then the structure may be polished to planarize the structure in some embodiments of the present invention.

Next, the recess 18 may be formed by dry or wet etching as indicated in Figure 4. For example, a dilute acid etchant is highly selective of metal (e.g., the electrode 16) over oxide (e.g., the insulator 12). For example, 60 to 80 percent sulfuric acid may be used with hydrogen peroxide and water. Another example, ammonia hydroxide may be used.

As shown in Figure 5, a layer of phase change material 20 may be deposited over the insulator 12 and filling the recess 18 in one embodiment of the present invention. As a result, in the stage shown in Figure 5, the phase change material 20 has a T-shaped configuration.

Turning next to Figure 6, a portion of the phase change material 20 overlying the insulator 12 may then be

removed by polishing, planarizing, or dry etching, to mention a few examples. As a result, a relatively small amount of phase change material 20a may be left by the damascene process in the region defined by the recess 18.

5        In some embodiments of the present invention, the phase change material 20a may constitute less than half the vertical extent of the heater 16. In one embodiment of the present invention, the phase change material 20a may constitute less than 25 percent of the overall vertical  
10 extent of the insulator 12. In another embodiment, the phase change material 20a may constitute about 10 percent or less of the vertical extent of the insulator 12.

Thereafter, an upper electrode 22 may be defined using suitable metal deposition techniques or any other technique  
15 well known to those skilled in the art.

In accordance with some embodiments of the present invention, the resulting cell involves phase change material that is confined to a relatively small volume of a pore. The phase change material may be encapsulated and  
20 isolated from the rest of the circuitry. In addition, in some embodiments, the phase change material is not part of the bitline. This reduces the need for an adhesion layer and reduces the amount of phase change material on the wafer surface in some embodiments. In addition, in some  
25 embodiments, all the volume of the phase change material is switched from one state to the other. Therefore, the bit

set resistance becomes saturated to a value independent of the programming current in the prior reset condition. This property may provide a reduced variation of set resistance across the bits. In addition, in some embodiments, current  
5 flows between two substantially parallel plate electrodes providing uniform current density.

Turning to Figure 8, a portion of a system 500 in accordance with an embodiment of the present invention is described. System 500 may be used in wireless devices such  
10 as, for example, a personal digital assistant (PDA), a laptop or portable computer with wireless capability, a web tablet, a wireless telephone, a pager, an instant messaging device, a digital music player, a digital camera, or other devices that may be adapted to transmit and/or receive  
15 information wirelessly. System 500 may be used in any of the following systems: a wireless local area network (WLAN) system, a wireless personal area network (WPAN) system, or a cellular network, although the scope of the present invention is not limited in this respect.

20 System 500 may include a controller 510, an input/output (I/O) device 520 (e.g. a keypad, display), a memory 530, and a wireless interface 540 coupled to each other via a bus 550. It should be noted that the scope of the present invention is not limited to embodiments having  
25 any or all of these components.

Controller 510 may comprise, for example, one or more microprocessors, digital signal processors, microcontrollers, or the like. Memory 530 may be used to store messages transmitted to or by system 500. Memory 530  
5 may also optionally be used to store instructions that are executed by controller 510 during the operation of system 500, and may be used to store user data. Memory 530 may be provided by one or more different types of memory. For example, memory 530 may comprise a volatile memory (any  
10 type of random access memory), a non-volatile memory such as a flash memory, and/or phase change memory that includes a memory element such as, for example, memory element 11 illustrated in Figure 1.

The I/O device 520 may be used to generate a message.  
15 The system 500 may use the wireless interface 540 to transmit and receive messages to and from a wireless communication network with a radio frequency (RF) signal. Examples of the wireless interface 540 may include an antenna, or a wireless transceiver, such as a dipole  
20 antenna, although the scope of the present invention is not limited in this respect.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and  
25 variations therefrom. It is intended that the appended

claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: